B. AMENDMENTS TO THE SPECIFICATION

Please amend the title at the top of the abstract on page 69 as follows:
~~Systm~~ System and Method for Manipulating Data Using a Plurality of Processors

Please amend the abstract on page 69, starting on line 4, as follows:
A system and a method for sharing a common system memory by a main processor and a plurality of secondary processors. The sharing of the common system memory enables the sharing of data between the processors. The data ~~are~~ is loaded into the common memory by the main processor, which divides the data to be processed into data blocks. The size of the data blocks ~~is~~ are equal to the size of the registers of the secondary processors. The main processor identifies an available secondary processor to process the first data block. The secondary processor processes the data block and returns the processed data block to the common system memory. The main processor may continue identifying available secondary processors and requesting the available secondary processors to process data blocks until all the data blocks have been processed.

Please amend the abstract on page 7, starting on line 7, as follows:
The data to be processed ~~are~~ is loaded into a common memory shared by a main processor and a plurality of secondary processors. The data may be loaded into the common memory by a main processor, which divides the data to be processed into data blocks. The size of the data blocks may be equal to the size of the registers of the secondary processors to facilitate processing of the data blocks by the secondary processors.

Please amend the paragraph on page 18, starting on line 25, as follows:
A plurality of BEs can be connected together in various configurations using such optical wave guides and the four optical ports of each BE. For example, as shown in **Figure 11B**, two or more BEs, e.g., BE **1152**, BE **1154** and BE **1156**, can be connected serially through such optical ports. In this example, optical interface **1166** of BE **1152** is connected through its optical ports to the optical ports of optical interface **1160** of BE **1154**. In a similar manner, the optical ports of optical

interface **1162** on BE **1154** are connected to the optical ports of optical interface **1164** of BE **1156.**

Please amend the paragraph on page 57, starting on line 21, as follows:

Figure 50 is a block diagram illustrating how the SPUs access the common memory to perform matrix operations on blocks of coefficients. **Figure 50** shows a system having ~~a main processor, PU **5010**, and~~ a number of secondary processors, such as SPU **5010**, SPU **5015**, SPU **5020**,..., and SPU **5025**. For example, SPU **5010** may be accessing block **5050**, SPU **5015** may be accessing block **5040**, SPU **5020** may be accessing block **5055**, and SPU **5025** may be accessing block **5045**. Blocks **5040, 5045, 5050,** and **5055** are located in common RAM **5035.**

Please amend the paragraph on page 5, starting on line 10, as follows:

Figure 2 is a diagram illustrating the structure of a processing element (PE) ~~processing unit (PU)~~ in accordance with the present invention;

Please amend the paragraphs, starting on page 12, line 28, through page 15, line 7, as follows:

The basic processing module for all members of network 104 is the ~~processing unit (PU)~~ processing element (PE). **Figure 2** illustrates the structure of a ~~PU~~ PE. As shown in this figure, ~~PU~~ PE 201 comprises a processing unit (PU) 203, a direct memory access controller (DMAC) 205 and a plurality of synergistic processing units (SPUs), namely, SPU 207, SPU 209, SPU 211, SPU 213, SPU 215, SPU 217, SPU 219 and SPU 221. A local ~~PU~~ PE bus 223 transmits data and applications among the SPUs, DMAC 205 and PU 203. Local ~~PU~~ PE bus 223 can have, e.g., a conventional architecture or be implemented as a packet switch network. Implementation as a packet switch network, while requiring more hardware, increases available bandwidth.

~~PU~~ PE 201 can be constructed using various methods for implementing digital logic. ~~PU~~ PE 201 preferably is constructed, however, as a single integrated circuit employing a complementary metal oxide semiconductor (CMOS) on a silicon substrate. Alternative materials for substrates include gallium arsinide, gallium aluminum arsinide and other so-called III-B compounds employing a wide variety of dopants. ~~PU~~ PE 201 also could be implemented using superconducting material, e.g., rapid single-flux-quantum (RSFQ) logic.

~~PU~~ PE 201 is closely associated with a dynamic random access memory (DRAM) 225 through a high bandwidth memory connection 227. DRAM 225 functions as the main memory for ~~PU~~ PE 201. Although a DRAM 225 preferably is a dynamic random access memory, DRAM 225 could be implemented using other means, e.g., as a static random access memory (SRAM), a magnetic random access memory (MRAM), an optical memory or a holographic memory. DMAC 205 facilitates the transfer of data between DRAM 225 and the SPUs and PU of ~~PU~~ PE 201. As further discussed below, DMAC 205 designates for each SPU an exclusive area in DRAM 225 into which only the SPU can write data and from which only the SPU can read data. This exclusive area is designated a "sandbox."

PU 203 can be, e.g., a standard processor capable of stand-alone processing of data and applications. In operation, PU 203 schedules and orchestrates the processing of data and applications by the SPUs. The SPUs preferably are single instruction, multiple data (SIMD) processors. Under the control of PU 203, the SPUs perform the processing of these data and applications in a parallel and independent manner. DMAC 205 controls accesses by PU 203 and the SPUs to the data and applications stored in the shared DRAM 225. Although ~~PU~~ PE 201 preferably includes eight SPUs, a greater or lesser number of SPUs can be employed in a ~~PU~~ PE depending upon the processing power required. Also, a number of ~~PUs~~ PEs, such as ~~PU~~ PE 201, may be joined or packaged together to provide enhanced processing power.

For example, as shown in **Figure 3**, four ~~PUs~~ PEs may be packaged or joined together, e.g., within one or more chip packages, to form a single processor for a member of network 104. This configuration is designated a broadband engine (BE). As shown in **Figure 3**, BE 301 contains four ~~PUs~~ PEs, namely, ~~PU~~ PE 303, ~~PU~~ PE 305, ~~PU~~ PE 307 and ~~PU~~ PE 309. Communications among these ~~PUs~~ PEs are over BE bus 311. Broad bandwidth memory connection 313 provides communication between shared DRAM 315 and these ~~PUs~~ PEs. In lieu of BE bus 311, communications among the ~~PUs~~ PEs of BE 301 can occur through DRAM 315 and this memory connection.

Input/output (I/O) interface 317 and external bus 319 provide communications between broadband engine 301 and the other members of network 104. Each ~~PU~~ PE of BE 301 performs processing of data and applications in a parallel and independent manner analogous to the parallel and independent processing of applications and data performed by the SPUs of a ~~PU~~ PE.

Please amend the paragraph on page 16, starting on line 17, as follows:

Figures 5-10 further illustrate the modular structure of the processors of the members of network 104. For example, as shown in **Figure 5**, a processor may comprise a single ~~PU~~ PE 502. As discussed above, this ~~PU~~ PE typically comprises a PU, DMAC and eight SPUs. Each SPU includes local storage (LS). On the other hand, a processor may comprise the structure of visualizer (VS) 505. As shown in **Figure 5**, VS 505 comprises PU 512, DMAC 514 and four SPUs, namely, SPU 516, SPU 518, SPU 520 and SPU 522. The space within the chip package normally occupied by the other four SPUs of a ~~PU~~ PE is occupied in this case by pixel engine 508, image cache 510 and cathode ray tube controller (CRTC) 504. Depending upon the speed of communications required for ~~PU~~ PE 502 or VS 505, optical interface 506 also may be included on the chip package.

Please amend the paragraph on page 17, starting on line 18, as follows:

The chip package of **Figure 8** comprises two ~~PUs~~ PEs 802 and 804 and two VSs 806 and 808. An I/O 810 provides an interface between the chip package and network 104. The output from the chip package is a video signal. This configuration may function as, e.g., a graphics work station.

Please amend the paragraph on page 17, starting on line 24, as follows:

Figure 9 illustrates yet another configuration. This configuration contains one-half of the processing power of the configuration illustrated in **Figure 8**. Instead of two ~~PUs~~ PEs, one ~~PU~~ PE 902 is provided, and instead of two VSs, one VS 904 is provided. I/O 906 has one-half the bandwidth of the I/O illustrated in **Figure 8**. Such a processor also may function, however, as a graphics work station.

Please amend the paragraph on page 18, starting on line 6, as follows:

Figure 11A illustrates the integration of optical interfaces into a chip package of a processor of network 104. These optical interfaces convert optical signals to electrical signals and electrical signals to optical signals and can be constructed from a variety of materials including, e.g., gallium arsinide, aluminum gallium arsinide, germanium and other elements or compounds. As shown in this figure, optical interfaces **1104** and **1106** are fabricated on the chip package of BE **1102**. BE bus **1108**

provides communication among the ~~PUs~~ PEs of BE **1102**, namely, ~~PU~~ PE **1110**, ~~PU~~ PE **1112**, ~~PU~~ PE **1114**, ~~PU~~ PE **1116**, and these optical interfaces. Optical interface **1104** includes two ports, namely, port **1118** and port **1120**, and optical interface **1106** also includes two ports, namely, port **1122** and port **1124**. Ports **1118**, **1120**, **1122** and **1124** are connected to, respectively, optical wave guides **1126**, **1128**, **1130** and **1132**. Optical signals are transmitted to and from BE **1102** through these optical wave guides via the ports of optical interfaces **1104** and **1106**.

Please amend the paragraph on page 24, starting on line 11, as follows:

As shown in **Figure 17**, one or more ~~PUs~~ PEs, e.g., ~~PU~~ PE **1720**, interact with DRAM **1702**. ~~PU~~ PE **1720** includes SPU **1722** and SPU **1740**. SPU **1722** includes control logic **1724**, and SPU **1740** includes control logic **1742**. SPU **1722** also includes local storage **1726**. This local storage includes a plurality of addressable memory locations **1728**. SPU **1740** includes local storage **1744**, and this local storage also includes a plurality of addressable memory locations **1746**. All of these addressable memory locations preferably are **1024** bits in size.

Please amend the paragraph on page 40, starting on line 28, as follows:

Figures 39, 40A and 40B illustrate the establishment of a dedicated pipeline structure comprising a group of SPUs and their associated sandboxes for the processing of streaming data, e.g., streaming MPEG data. As shown in **Figure 39**, the components of this pipeline structure include ~~PU~~ PE **3902** and DRAM **3918**. ~~PU~~ PE **3902** includes PU **3904**, DMAC **3906** and a plurality of SPUs, including SPU **3908**, SPU **3910** and SPU **3912**. Communications among PU **3904**, DMAC **3906** and these SPUs occur through ~~PU~~ PE bus **3914**. Wide bandwidth bus **3916** connects DMAC **3906** to DRAM **3918**. DRAM **3918** includes a plurality of sandboxes, e.g., sandbox **3920**, sandbox **3922**, sandbox **3924** and sandbox **3926**.